

FIG. 2A is a schematic diagram of a system 100 for generating a signal. The system 100 includes a processor 102, a memory 104, and a transmitter 106. The processor 102 is configured to generate a signal and control the transmitter 106 to transmit the signal. The memory 104 is configured to store data and instructions. The transmitter 106 is configured to transmit the signal over a communication channel 108. The system 100 may be implemented in a variety of devices, including a mobile phone, a laptop computer, or a server.

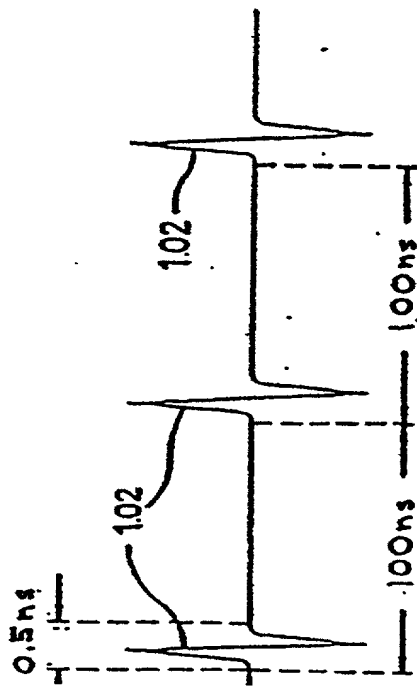


FIG. 2A

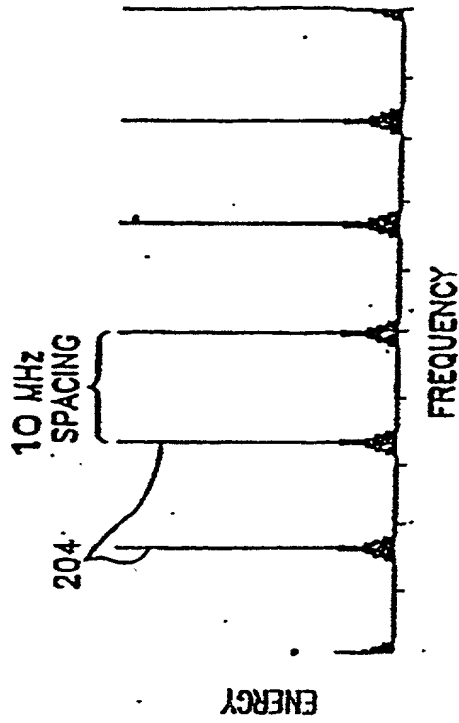


FIG. 2B

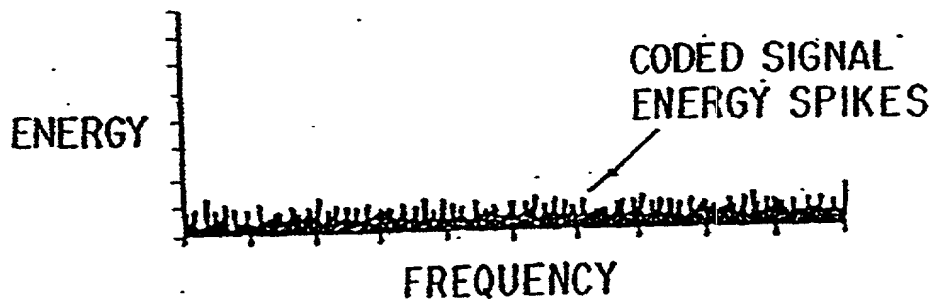


FIG. 3

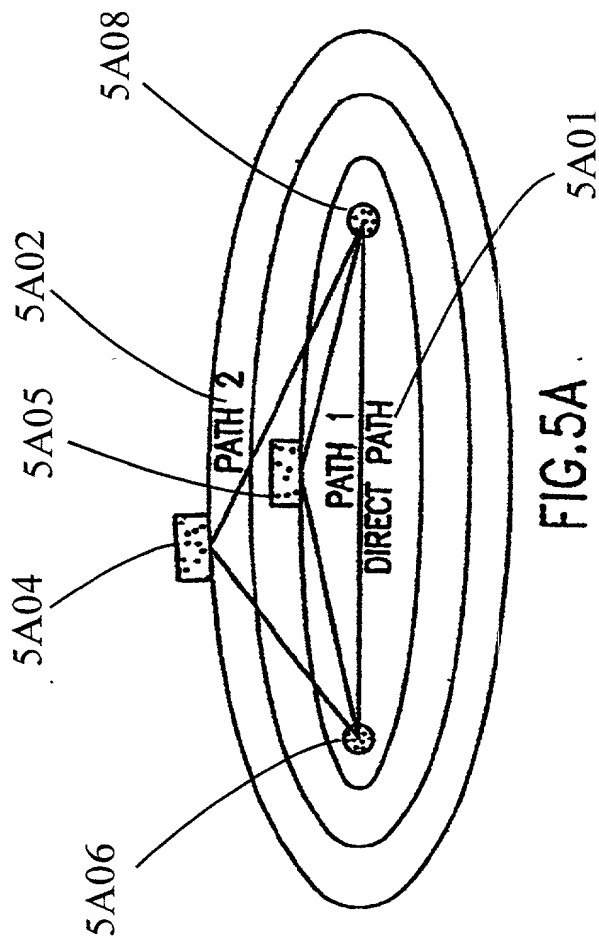


FIG. 5A

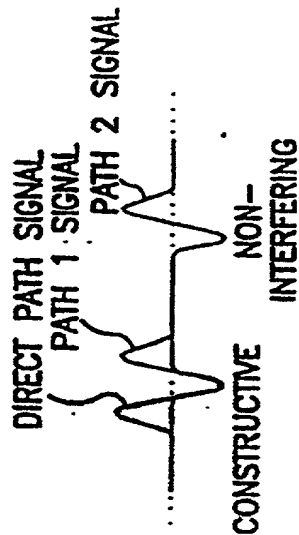
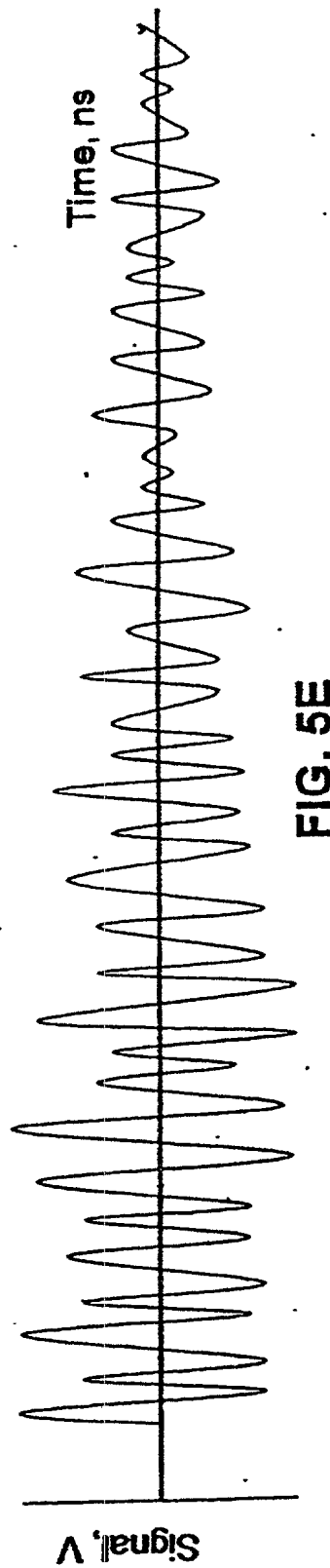
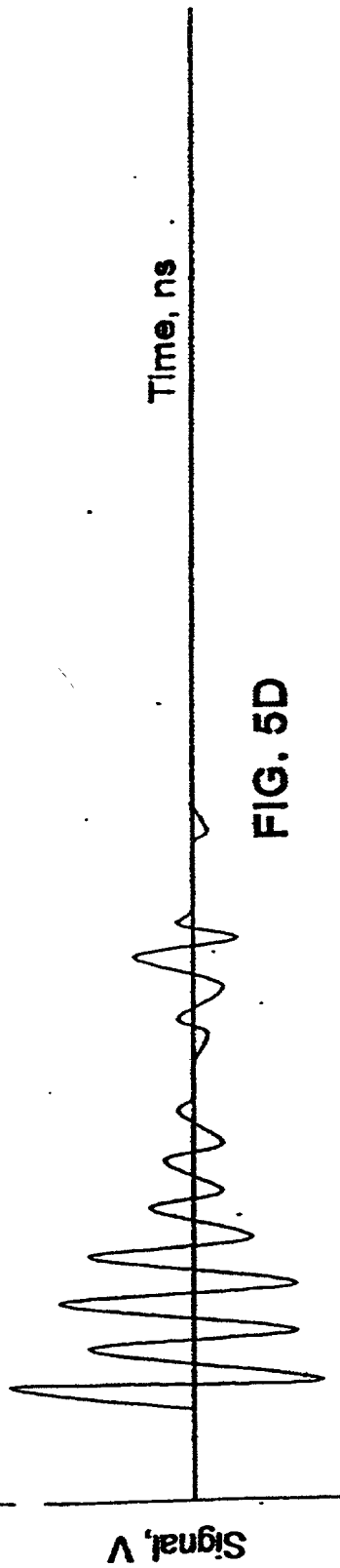
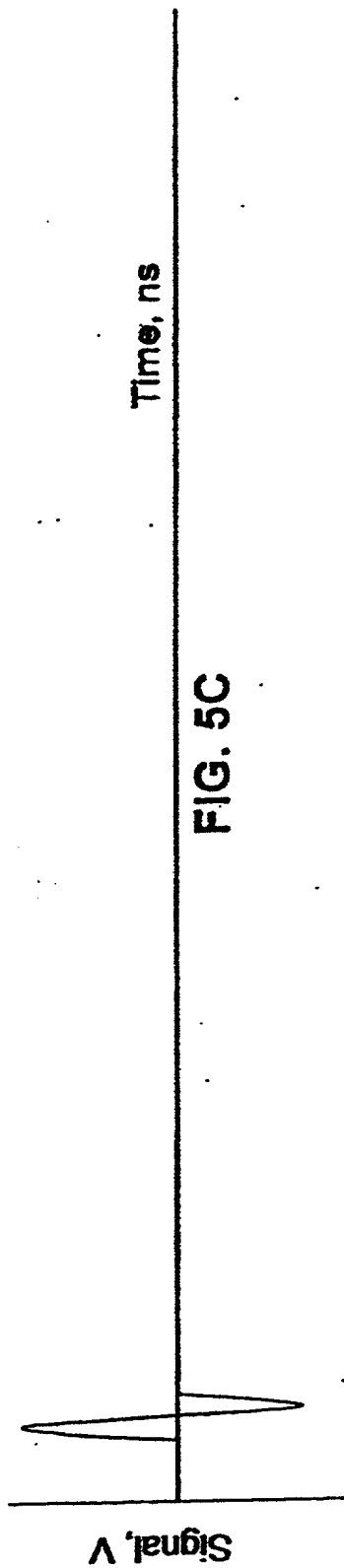


FIG. 5B



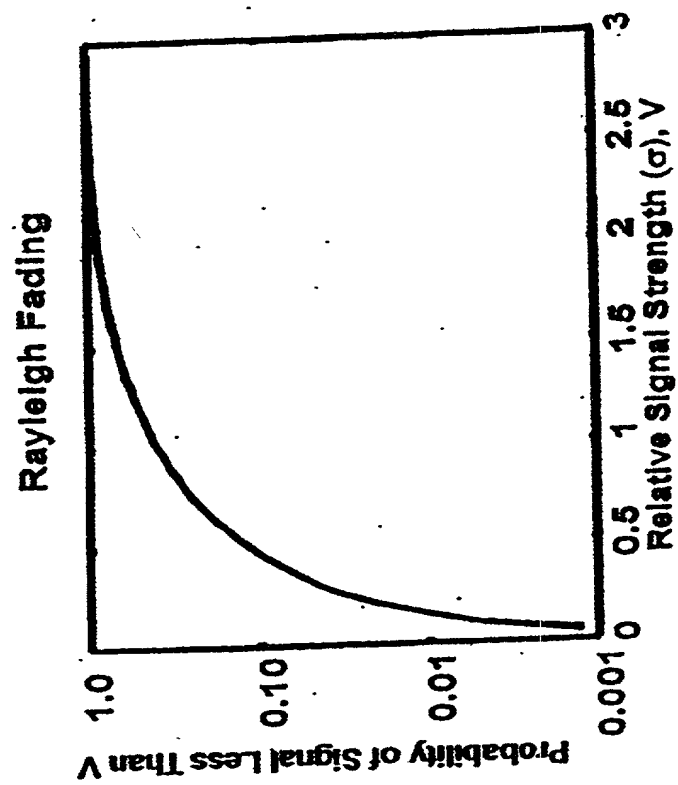


Fig. 5.

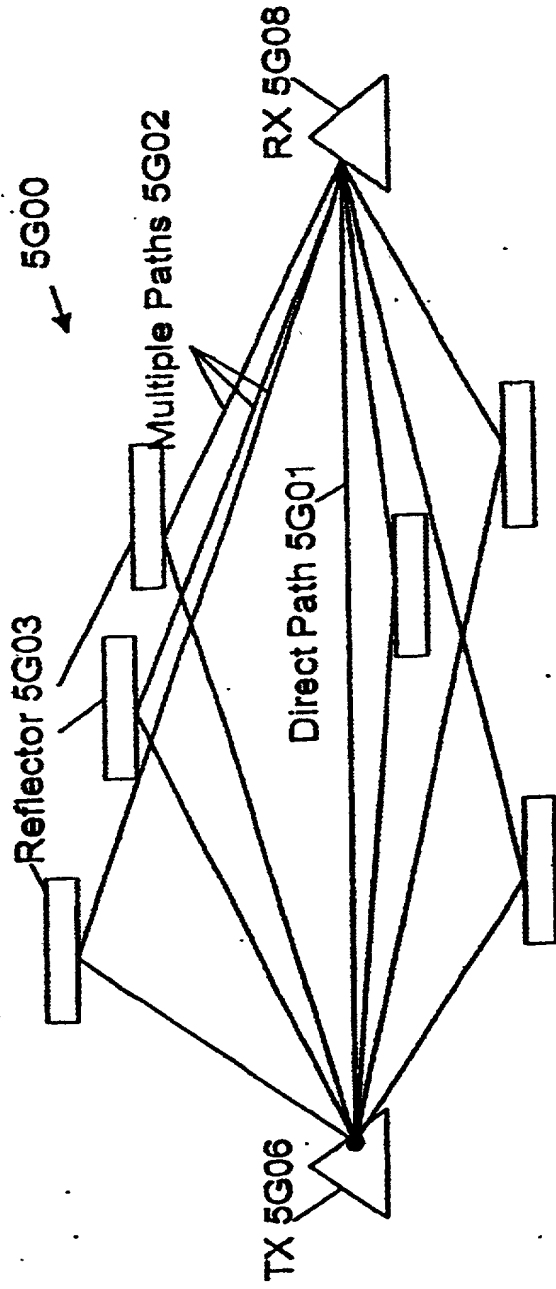


FIG. 5G

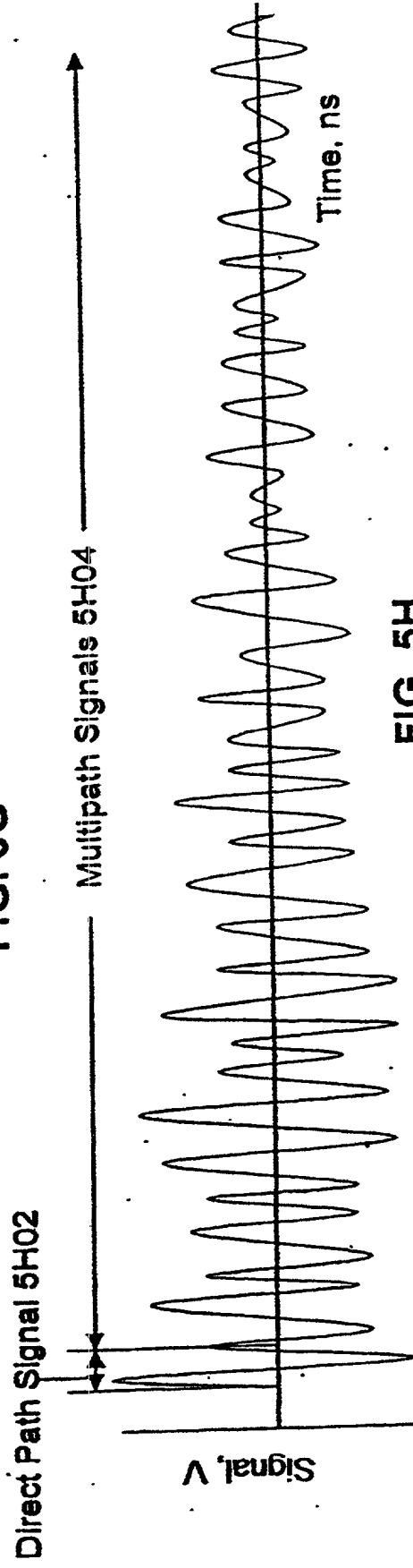
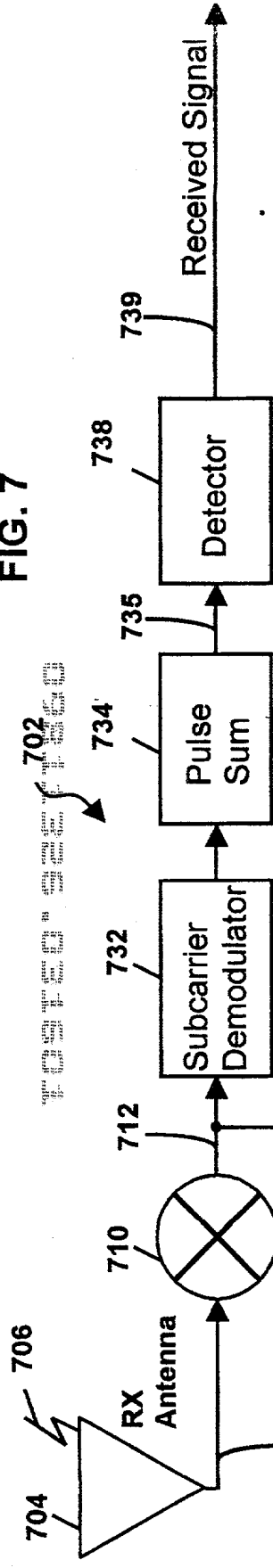


FIG. 7



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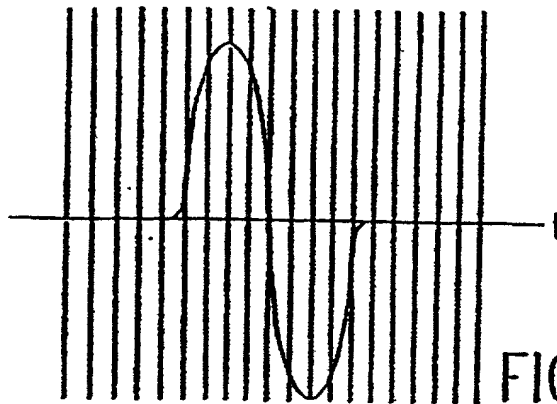


FIG. 8A

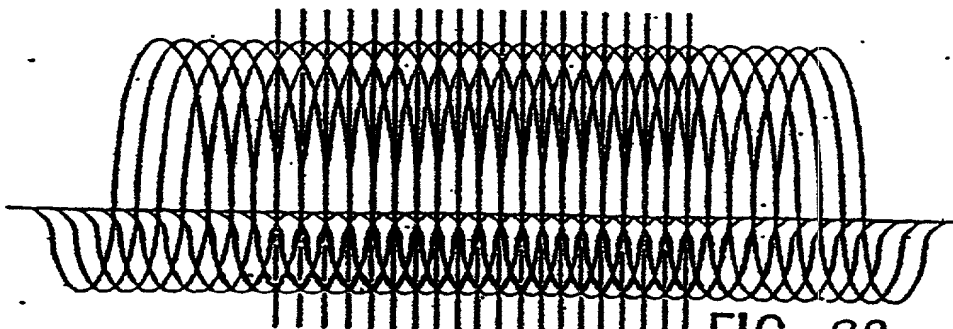
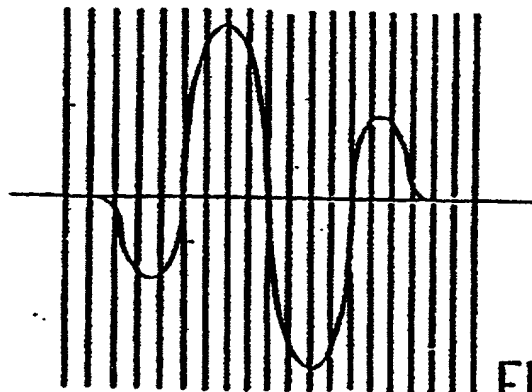


FIG. 8B



CORRESPONDING
TO EACH
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FIG. 8C

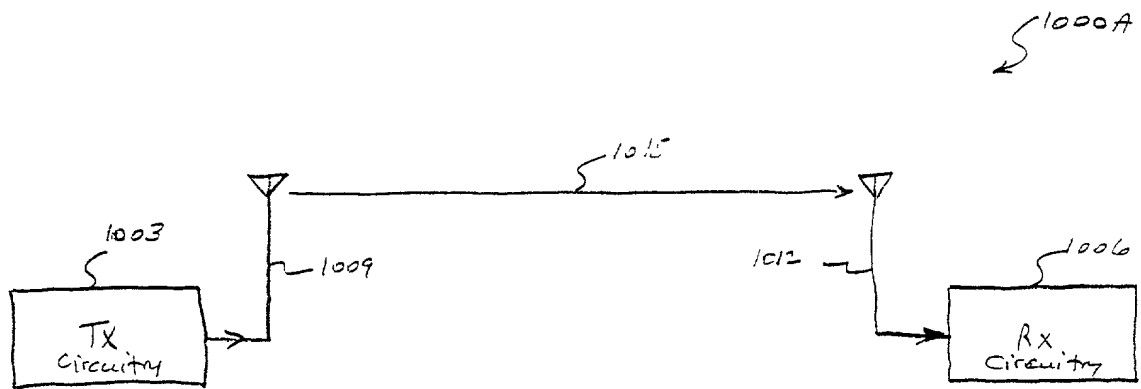


FIG. 9

FIG. 10A

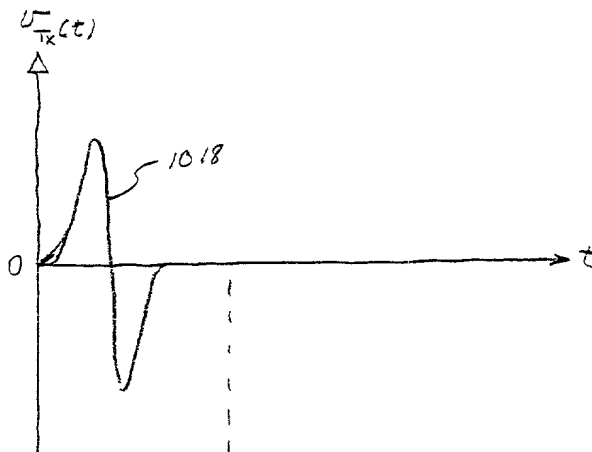
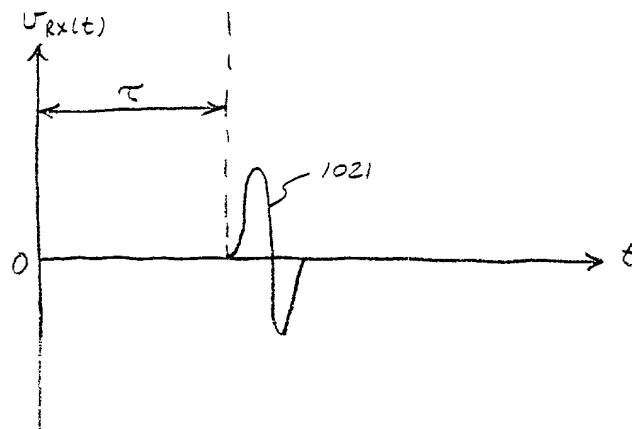


FIG. 10B



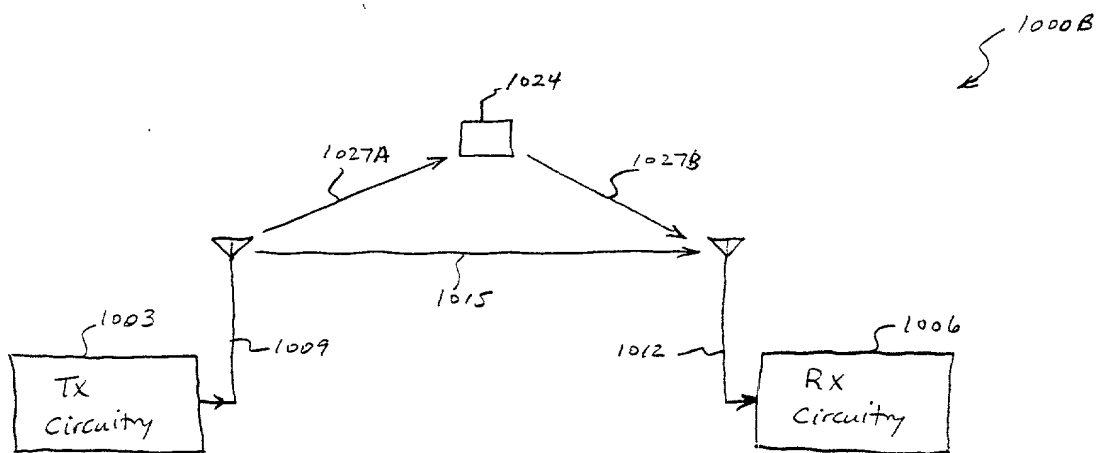
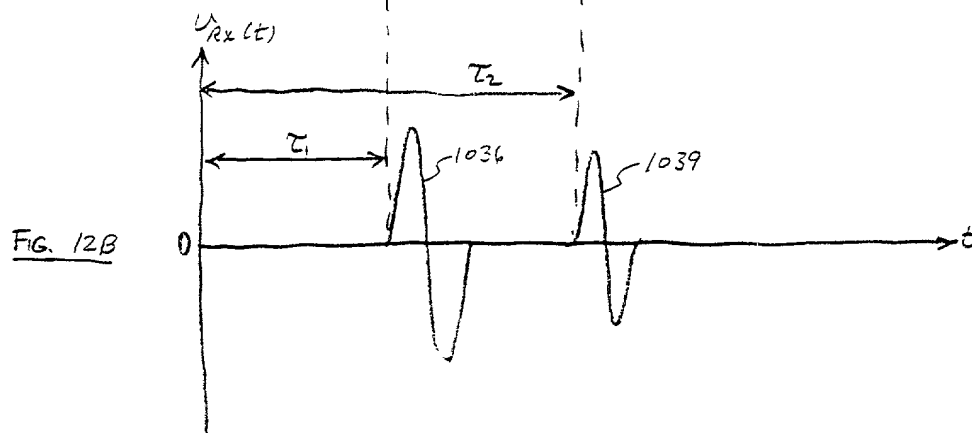
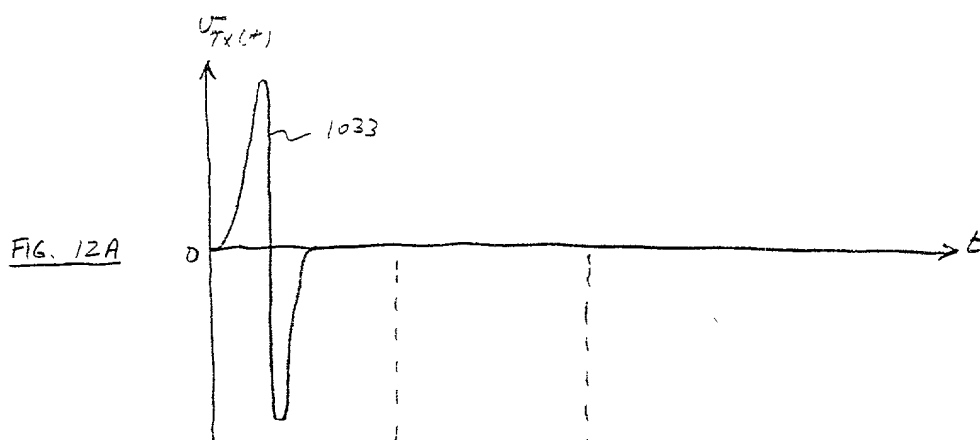


FIG. 11



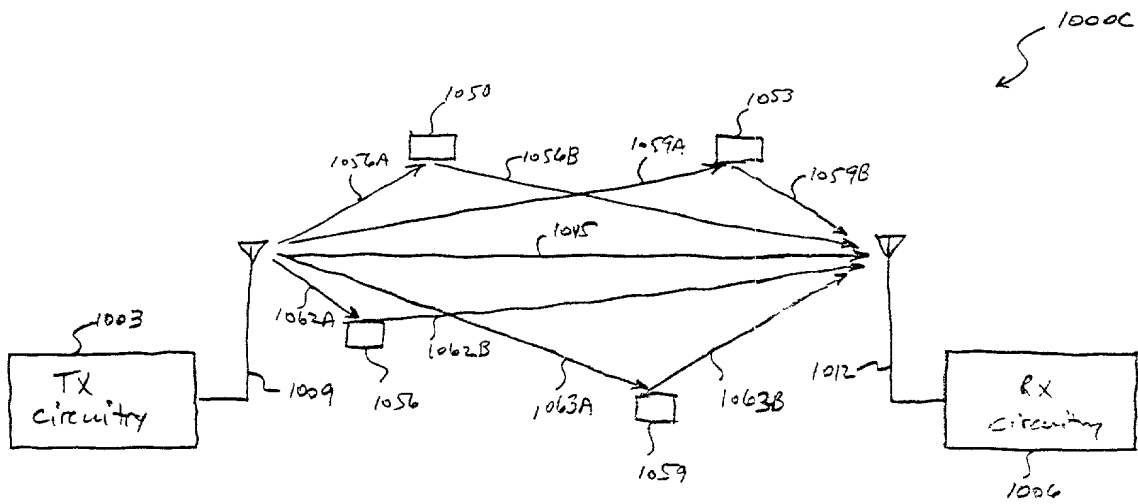
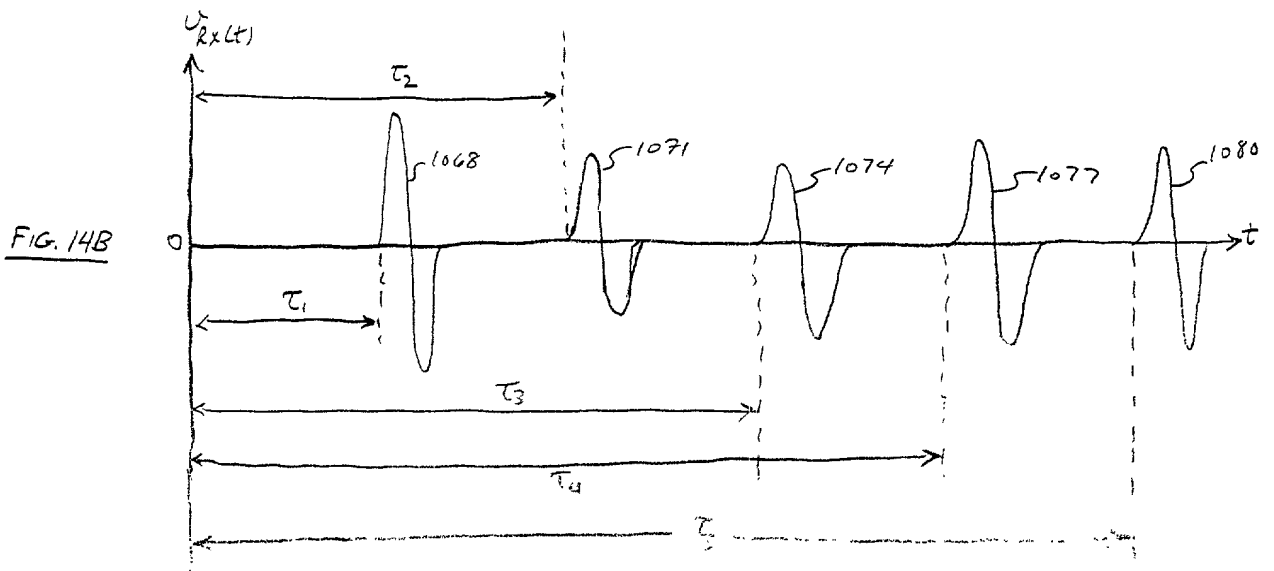
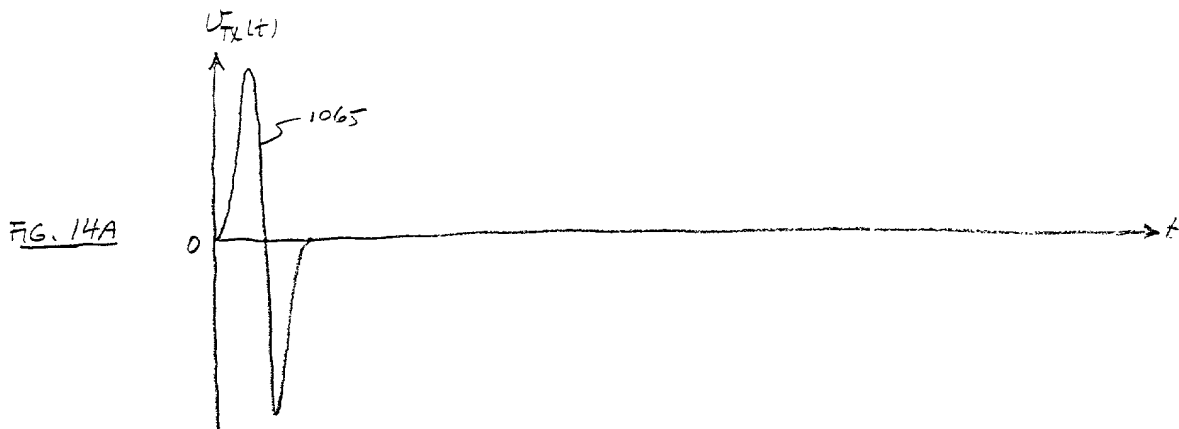
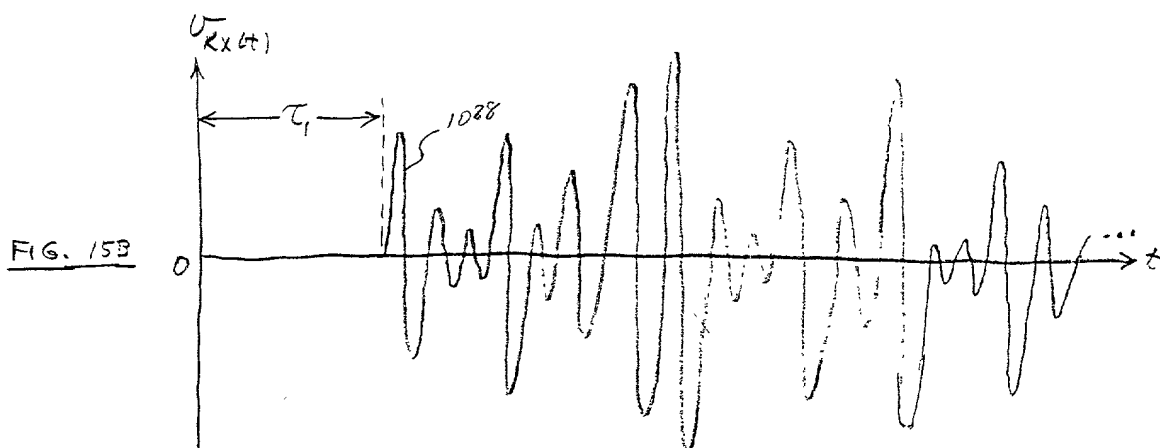
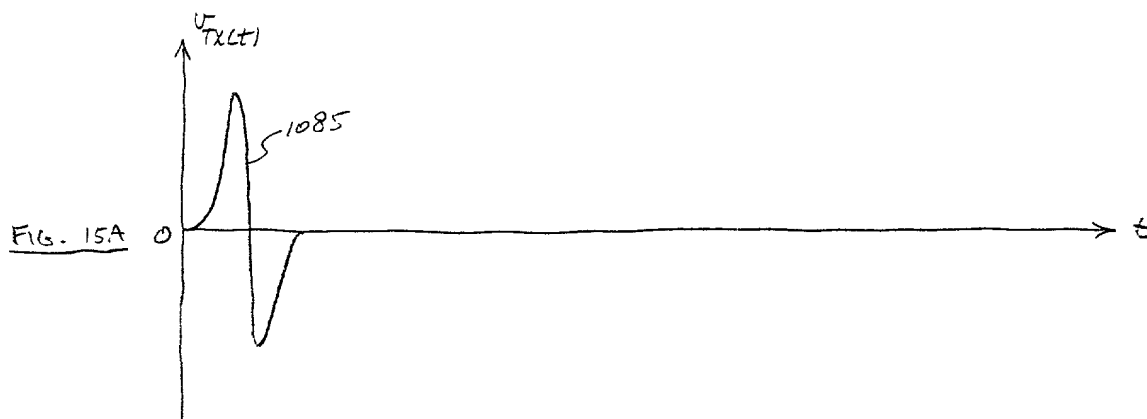


FIG. 13





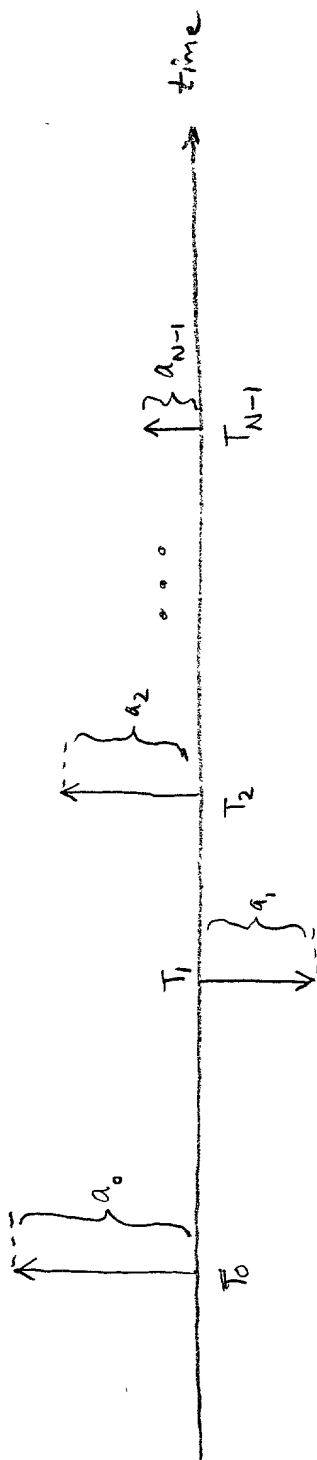


FIG. 16

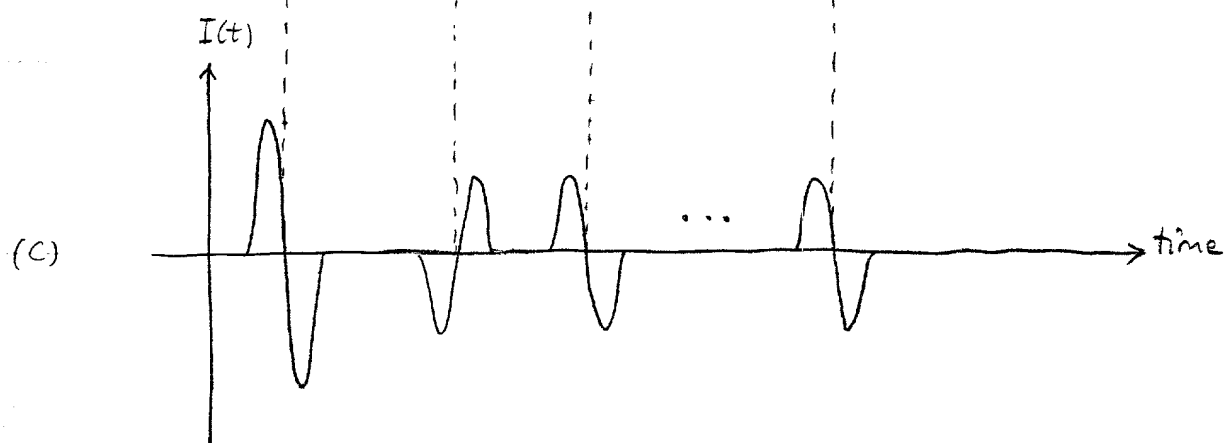
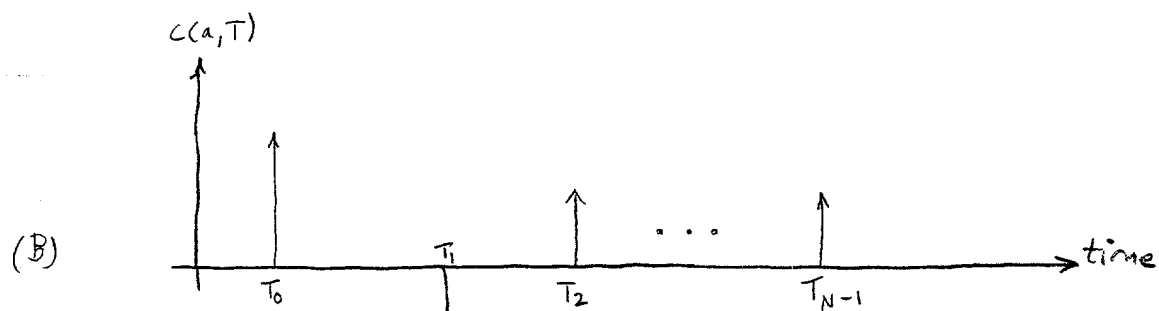
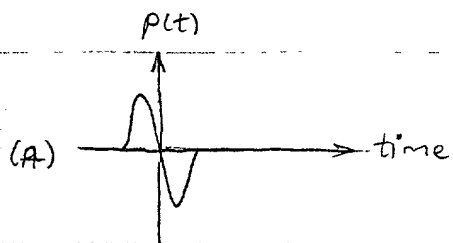


FIG. 17

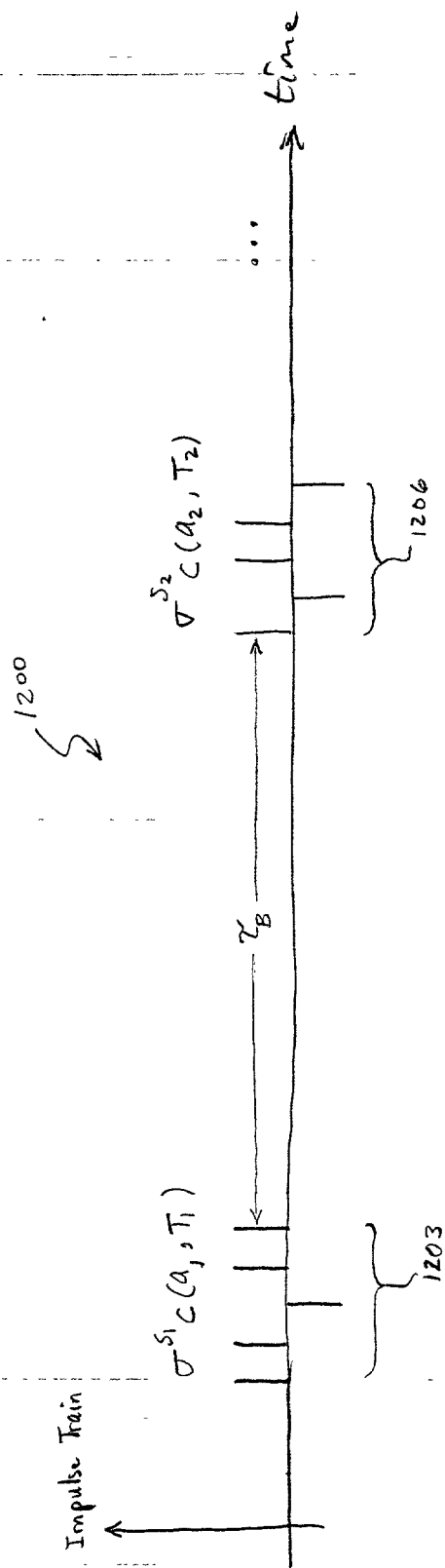


FIG. 18

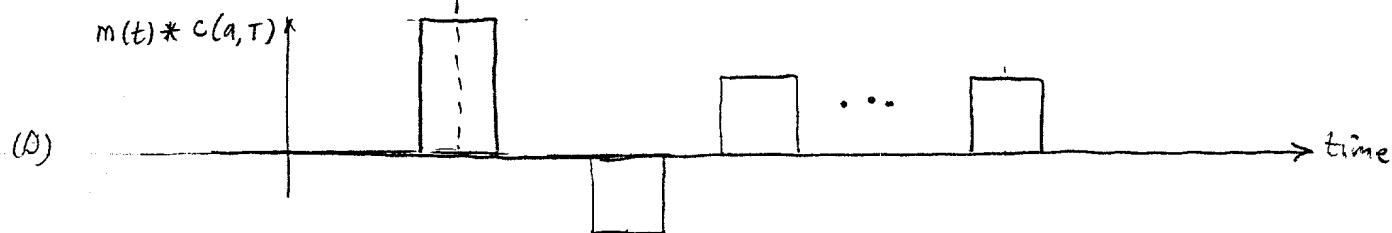
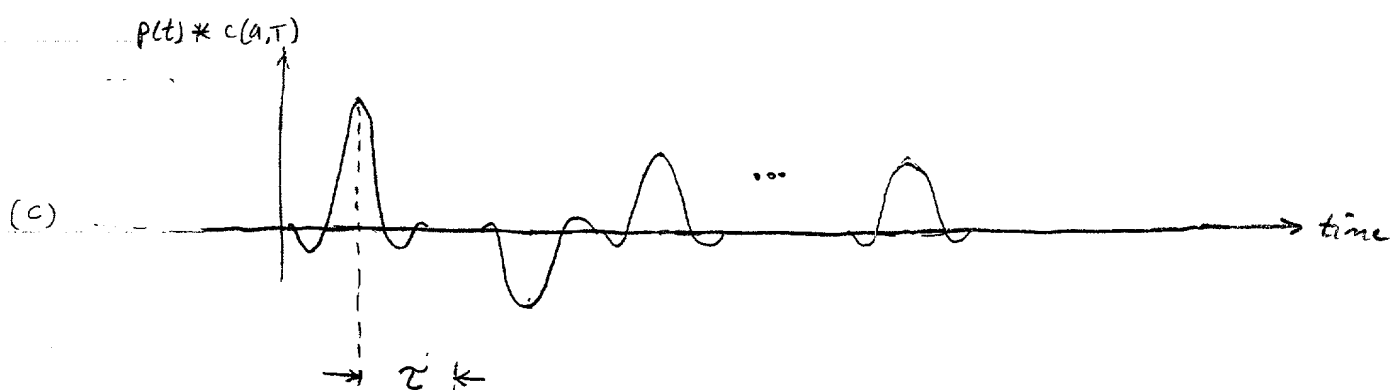
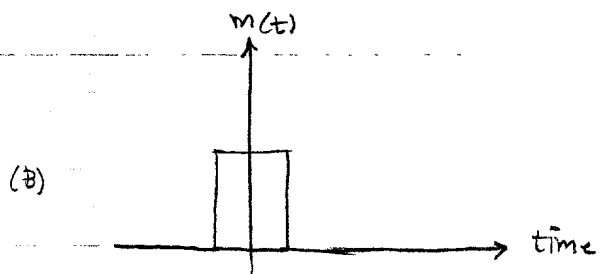
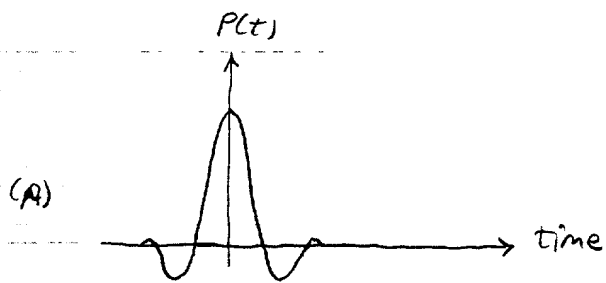


FIG. 19

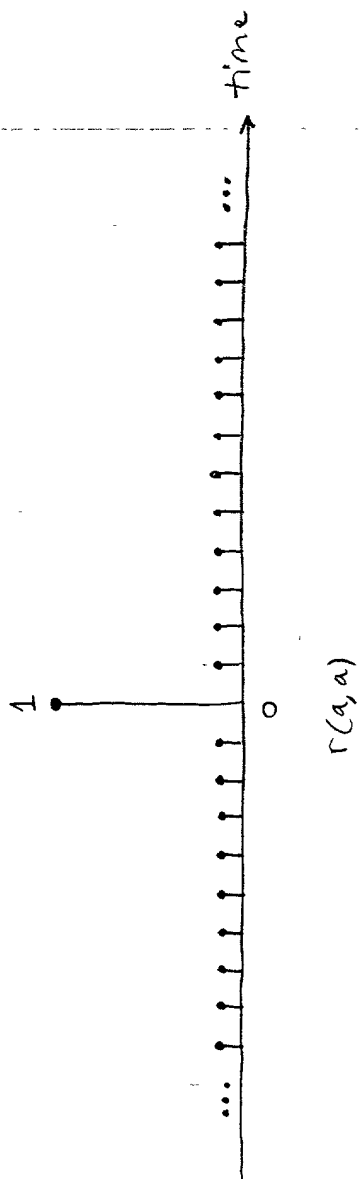
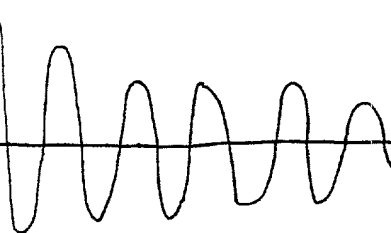


FIG. 20

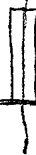
$p(t)$



time

(A)

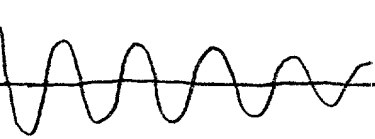
$m(t)$



time

(B)

$R(p(t), m(t))$

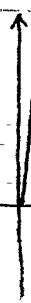


time

(C)

FIG. 21

$p(t)$



time

(A)

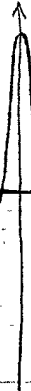
$m(t)$



time

(B)

$R(p(t), m(t))$



time

(C)

FIG. 22

1. The first part of the figure shows a sequence of vertical lines of varying heights, representing a discrete-time signal. The horizontal axis is labeled "time". The vertical axis is labeled $C_B(a, T)$. The lines are centered around a horizontal line, with some lines extending above and some below. The heights of the lines vary, with some being significantly taller than others. The lines are spaced evenly along the horizontal axis.

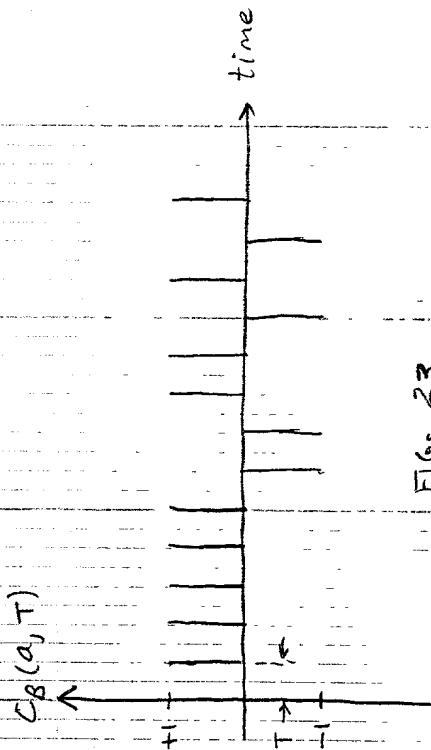


FIG. 23

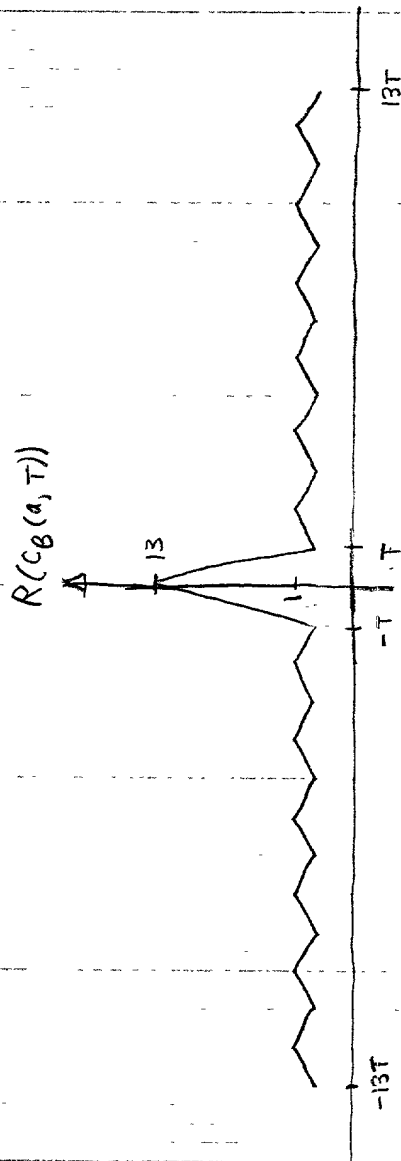


FIG. 24

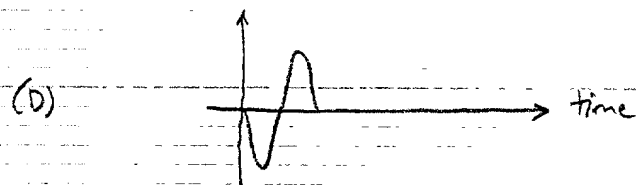
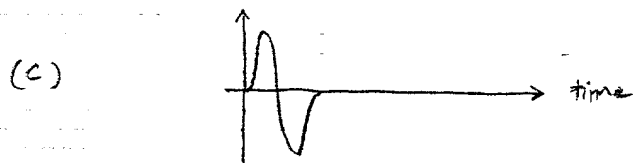
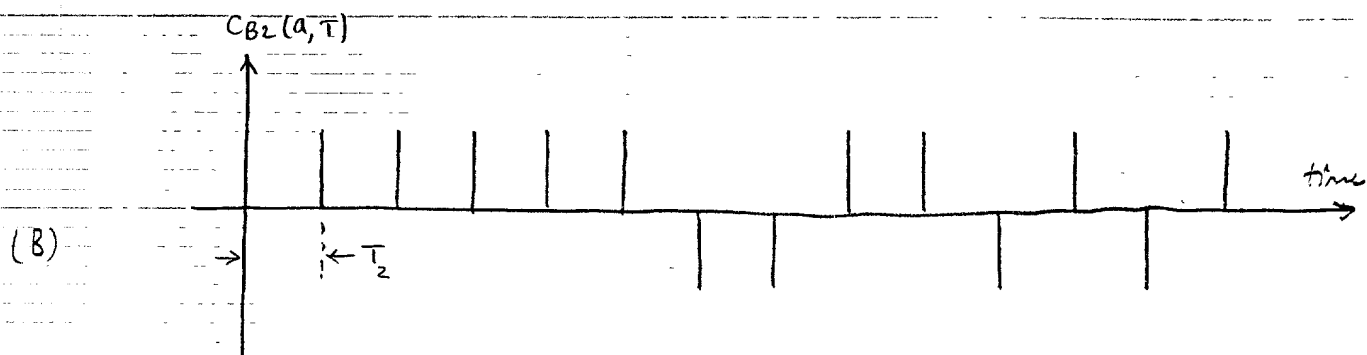
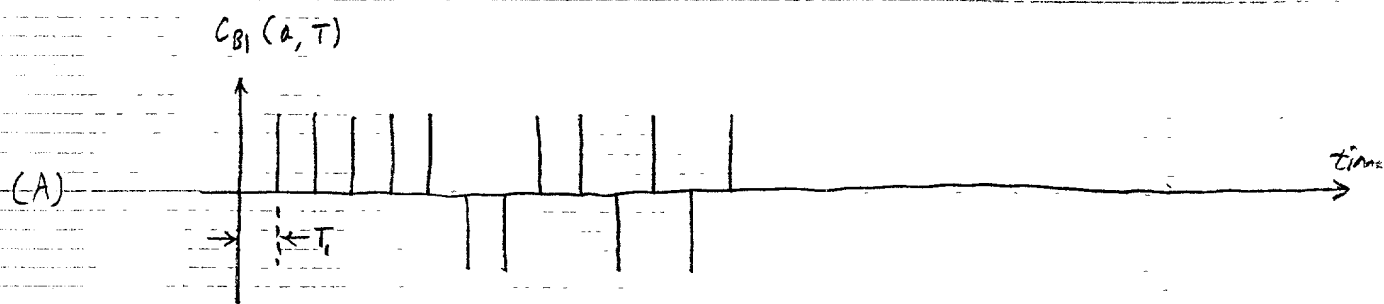


FIG. 25

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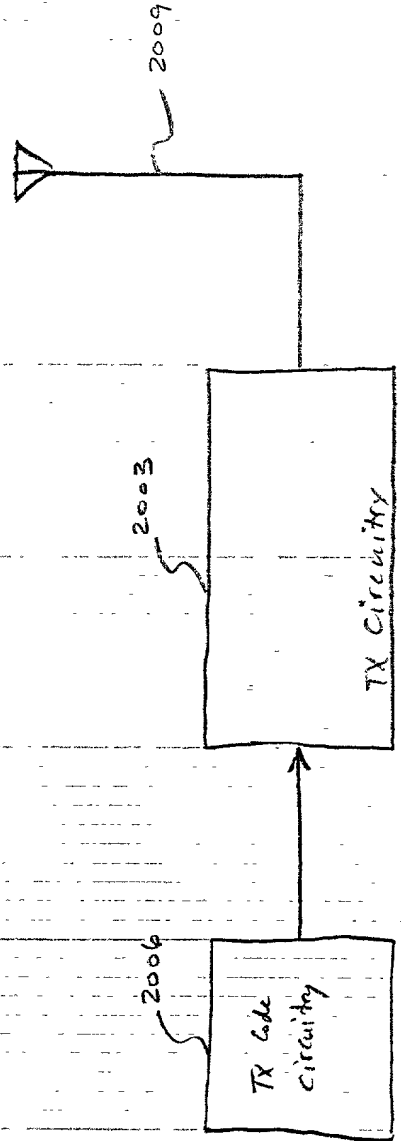


FIG. 26

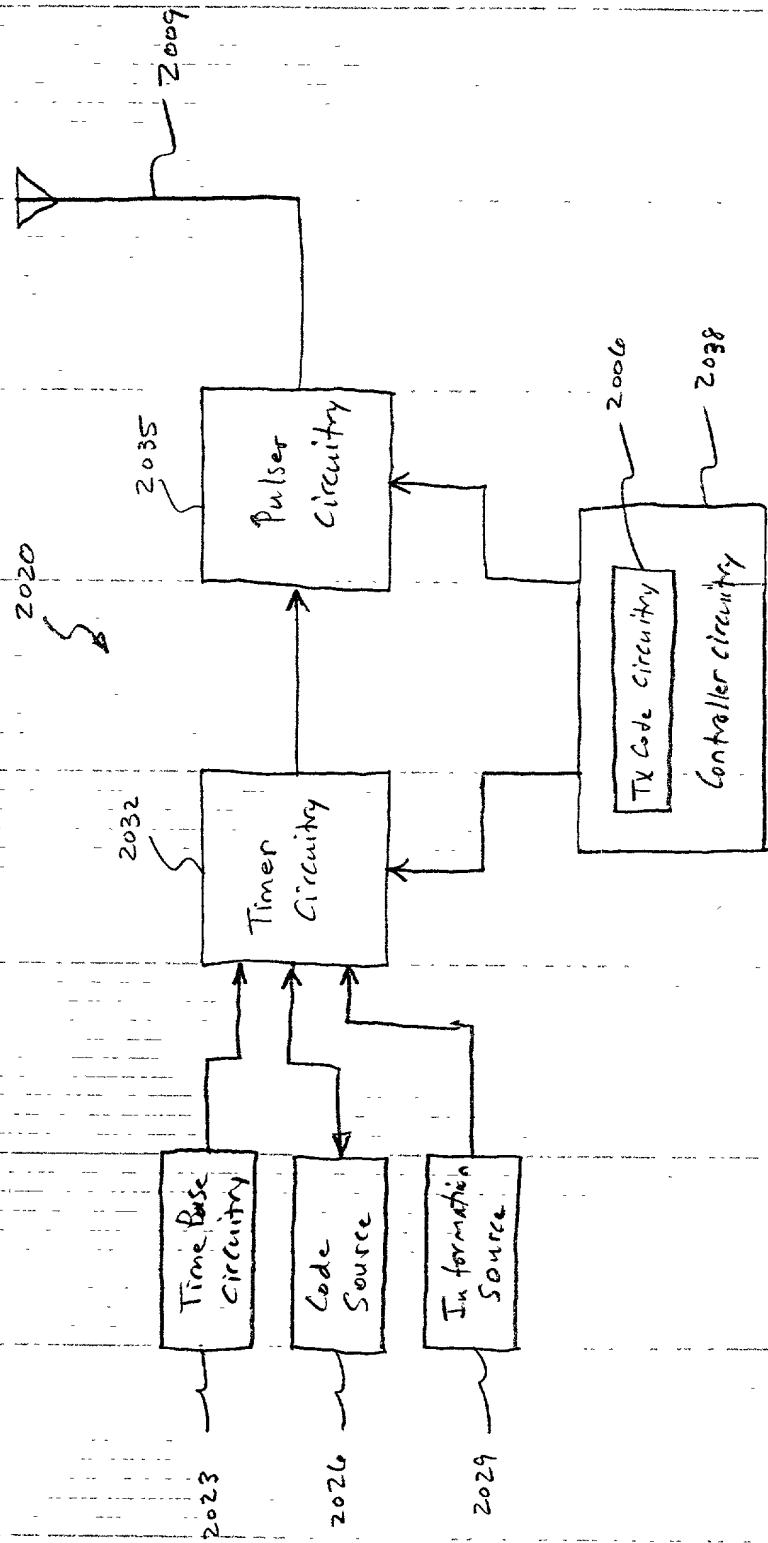


FIG. 27A

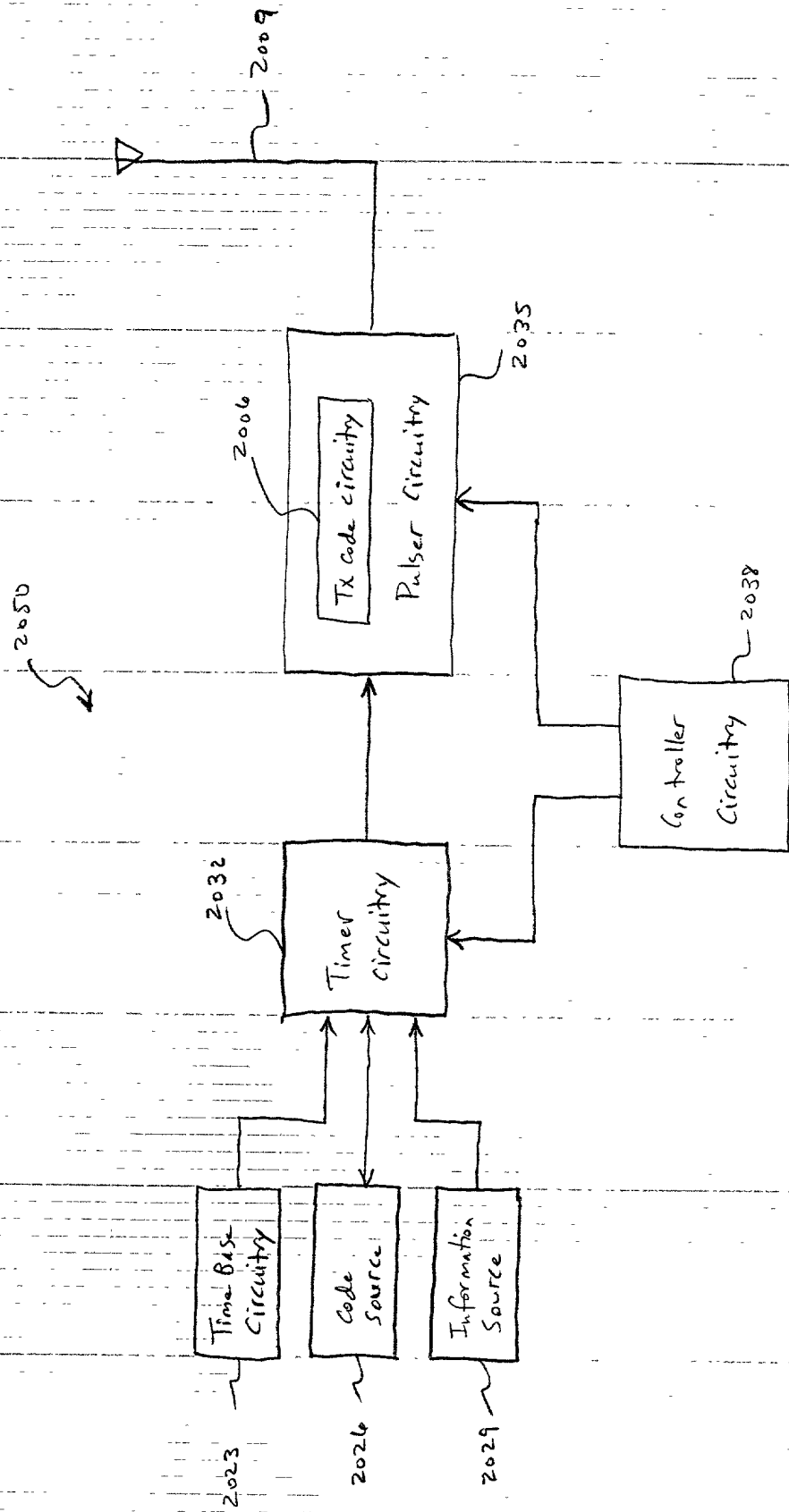


FIG. 27B

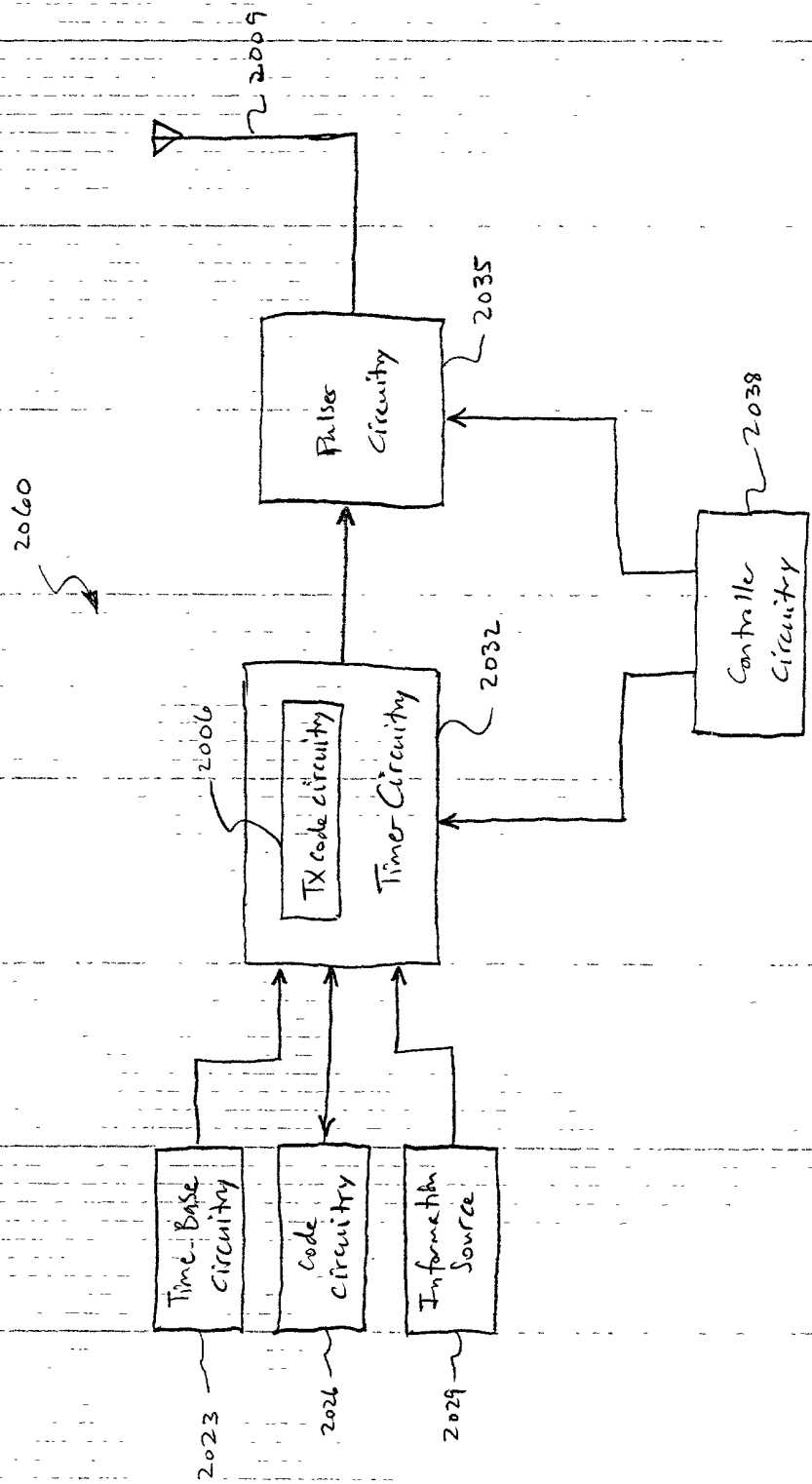


FIG. 27C

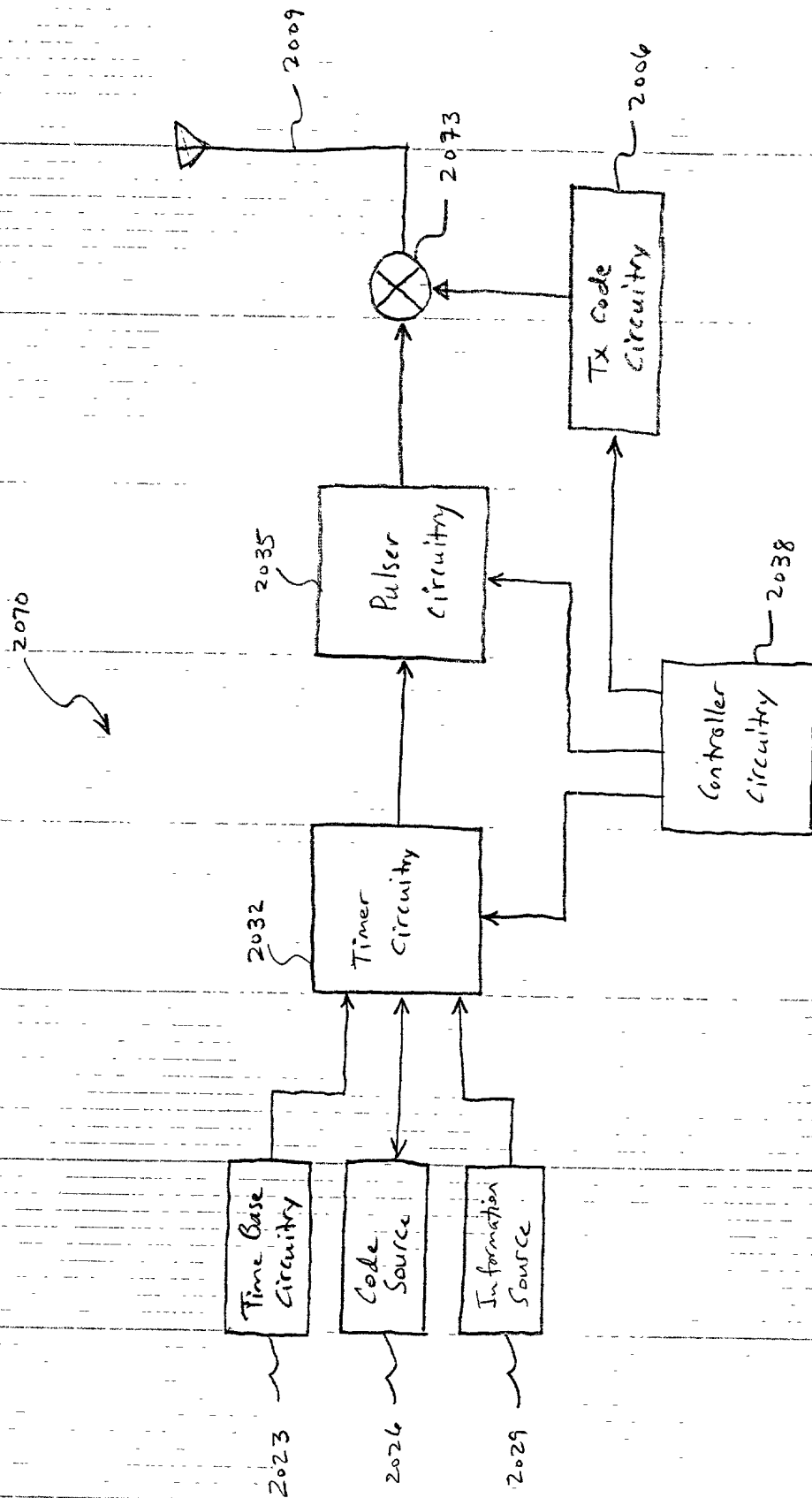


FIG. 27D

FIG. 28A is a block diagram of a receiver system 2100. The system includes an antenna 2109, RX circuitry 2103, and RX code circuitry 2106. The antenna 2109 is connected to the RX circuitry 2103, which is in turn connected to the RX code circuitry 2106.

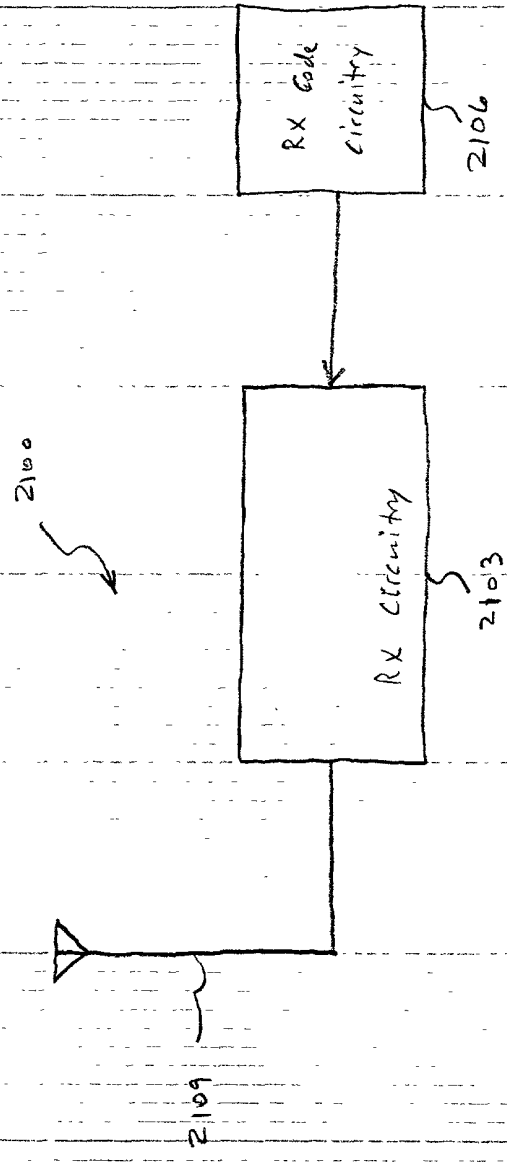


FIG. 28A

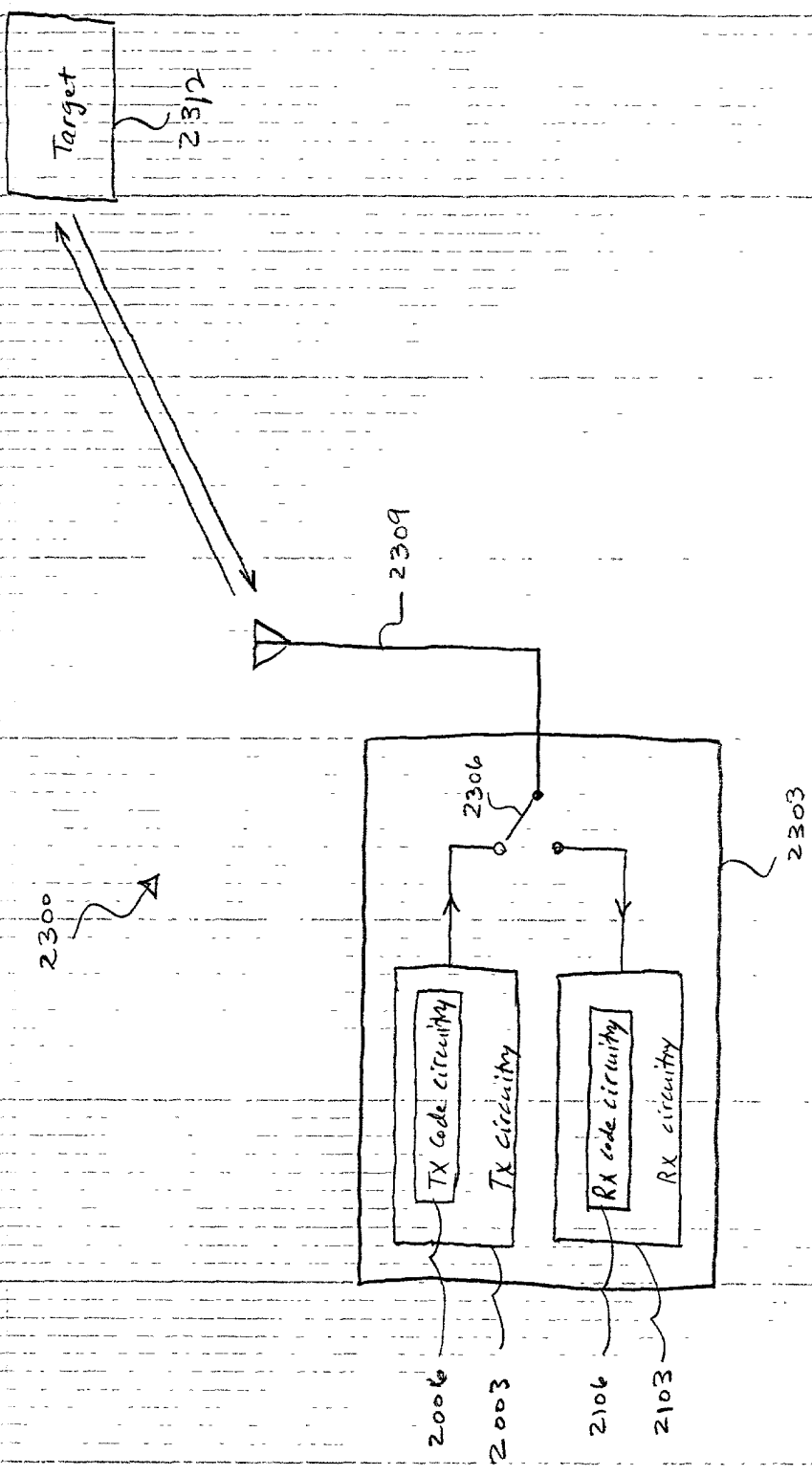


FIG. 29A

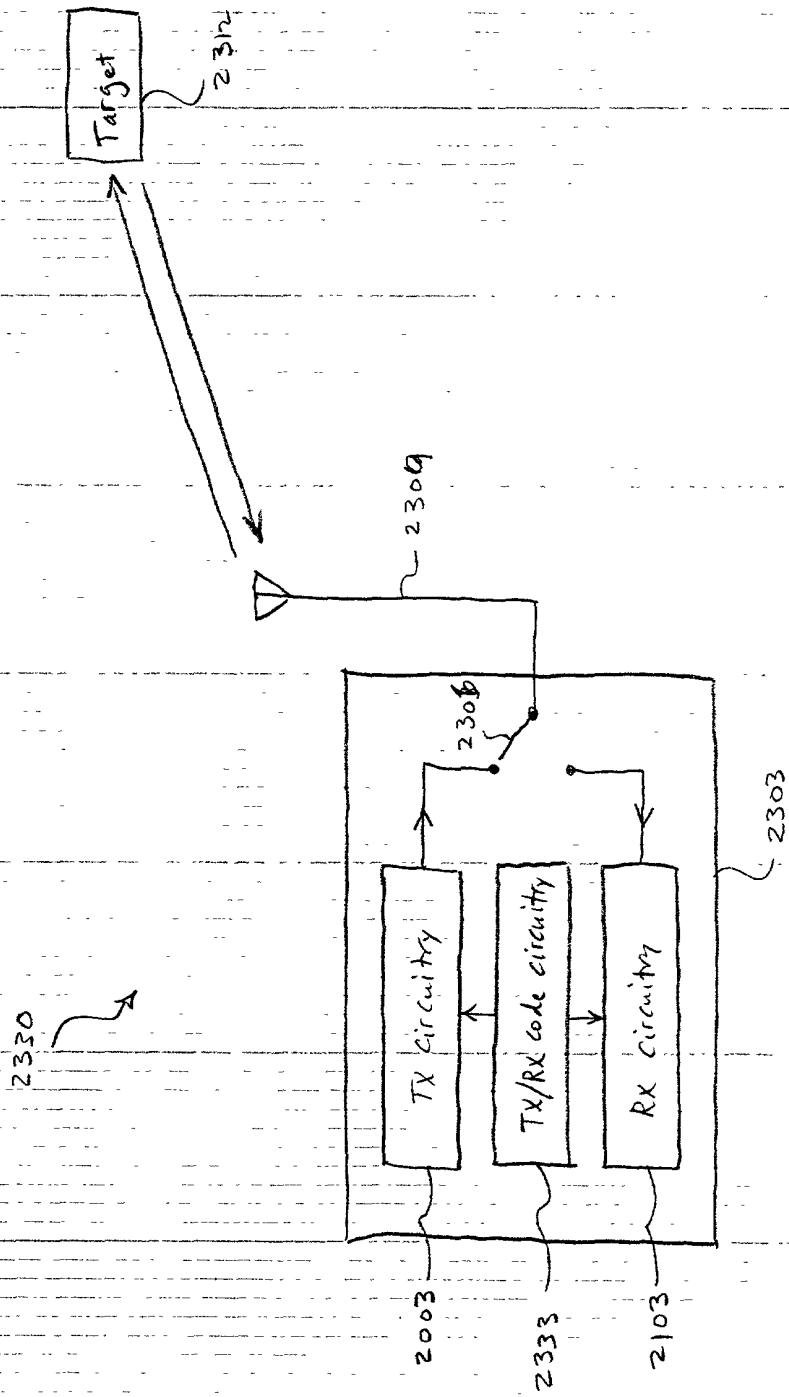


FIG. 29B

2340

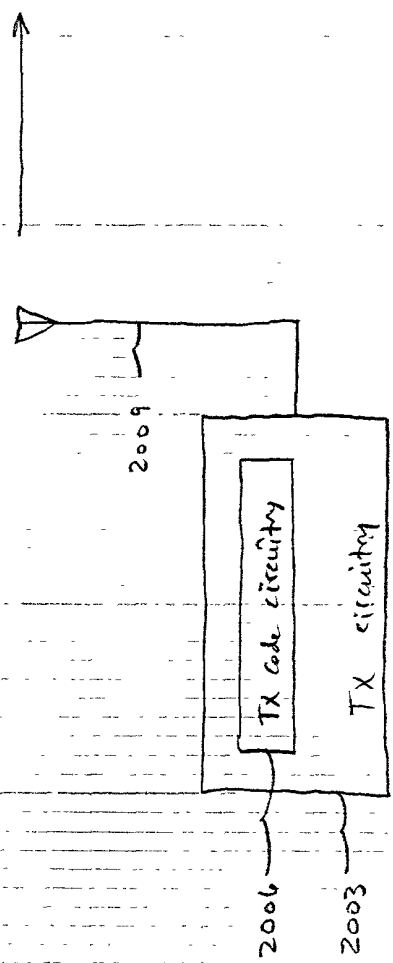
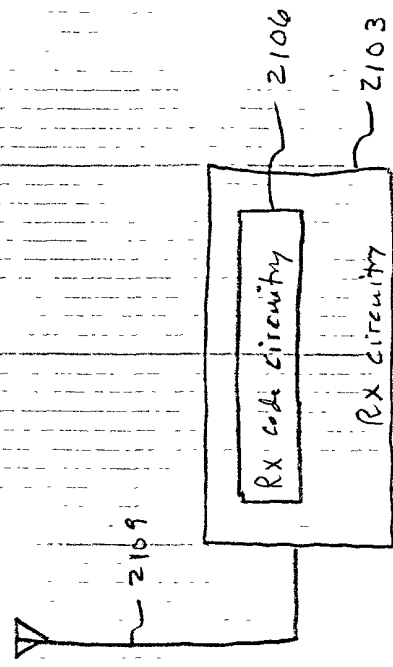


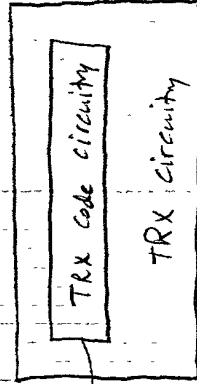
FIG. 30

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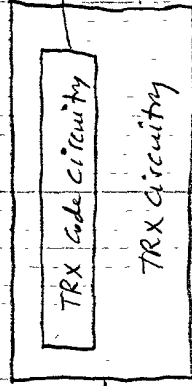
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FIG. 31A

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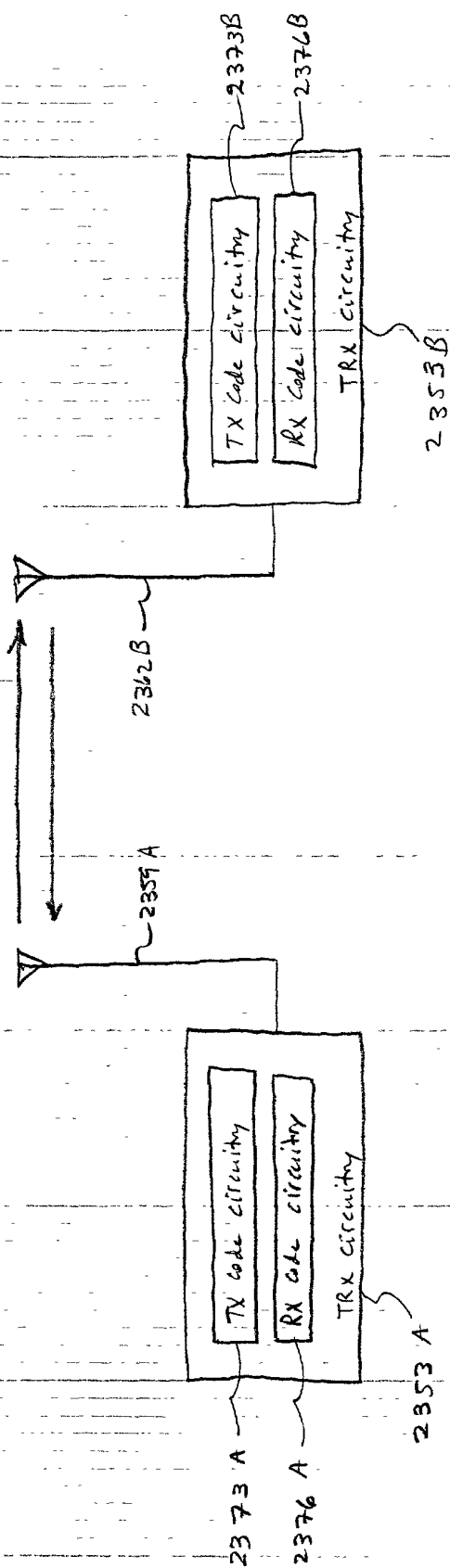


FIG. 31B